

# **Digital Logic Experiment Report (1** )

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| **Digital Logic Experiment 1** | | |
| **1. Design of a series of binary adders 50%** | **2. Small laboratory access control system design 50%** | **Overall result** |
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评语：（包含：预习报告内容、实验过程、实验结果及分析）

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**Digital Logic Lab Report**

Serial Binary Adder Design Preview Report

1. Design of a series of binary adders

1. Experiment name

Serial binary adder design .

2. The purpose of the experiment

The students are required to use the traditional circuit design method to design five kinds of binary adders , and use tool software, for example, the virtual simulation function of " logisim " software to check whether the circuit design meets the requirements .

Through the three training processes of design , simulation, and verification of the above experiments , students can master the methods of design, simulation, and debugging of traditional logic circuits .

3. Equipment used in the experiment

of Logisim 2.7.1 software .

4. Experimental content

For the five kinds of binary adders that have been designed , use logisim software to carry out virtual experiment simulation on them . Except for logic gates and flip-flops, the logic library components provided by logisim software cannot be used directly. The specific content is as follows.

**(1) One bit binary half adder**

half adder, the circuit has two inputs A , B , two outputs S and C. Inputs A and B are the summand and addend respectively, and the outputs S and C are the basic sum and carry to the high order.

**(2) One-bit binary full adder**

Design a one-bit binary full adder, the circuit has three inputs A , B and C i , and two outputs S and C o . The input A , B and C i are the summand, the addend and the carry from the lower bit respectively, and the output S and C o are the original bit and the carry to the higher bit.

**(3) Four-bit binary parallel adder with serial carry**

Use four one-bit binary full adders in series to design a four-bit binary parallel adder with serial carry. The circuit has nine inputs A 3 , A 2 , A 1 , A 0 , B 3 , B 2 , B 1 , B 0 and C 0 , five outputs S 3 , S 2 , S 1 , S 0 and C 4 . Input A= A 3 A 2 A 1 A 0 , B= B 3 B 2 B 1 B 0 and C 0 are summand, addend and carry from low bit respectively, output S= S 3 S 2 S 1 S 0 And C o is the standard and the carry to the high position.

**( 4) Four-bit binary parallel adder with carry first**

Using the idea of forward carry to design a four-bit binary parallel adder with advanced carry, the circuit has nine inputs A 3 , A 2 , A 1 , A 0 , B 3 , B 2 , B 1 , B 0 and C 0 , Five outputs S 3 , S 2 , S 1 , S 0 and C 4 . Input A= A 3 A 2 A 1 A 0 , B= B 3 B 2 B 1 B 0 and C 0 are summand, addend and carry from low bit respectively, output S= S 3 S 2 S 1 S 0 And C o is the standard and the carry to the high position.

**(5) Encapsulate the four-bit binary parallel adder with carry forward into a component and verify its correctness**

Encapsulate the designed four-bit binary parallel adder with carry forward, generate a " private " library component and verify its correctness for subsequent experiments. The encapsulated logic symbols are shown in Figure 1-1.

**S3 S2 S1 S0**

**C4 四位二进制并行加法器 C0**

**A3 A2 A1 A0  B3 B2 B1 B0**

Figure 1-1 " Private " carry-ahead four-bit binary parallel adder

5. Experimental program design

**(1) Design scheme of a binary half adder**

Table 1-1 is a binary half adder truth table.

Table 1 -1 Truth table of a binary half adder

|  |  |  |  |
| --- | --- | --- | --- |
| enter | | output | |
| A | B | C | S |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

It can be seen from the table that S=/AB+A/B =A ⊕B, C=AB. According to this, the logic circuit of a binary half adder can be designed in Logisim .

Figure 1-2 is a binary half adder.

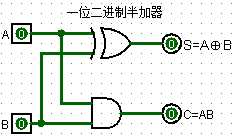


Figure 1-2 One bit binary half adder

**(2) Design scheme of a binary full adder**

Table 1-2 is a binary full adder truth table.

Table 1 -2 Truth table of a binary full adder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| enter | | | output | | |
| C 1 | A | B | | S | C 0 |
| 0 | 0 | 0 | | 0 | 0 |
| 0 | 0 | 1 | | 1 | 0 |
| 0 | 1 | 0 | | 1 | 0 |
| 0 | 1 | 1 | | 0 | 1 |
| 1 | 0 | 0 | | 1 | 0 |
| 1 | 0 | 1 | | 0 | 1 |
| 1 | 1 | 0 | | 0 | 1 |
| 1 | 1 | 1 | | 1 | 1 |

It can be known from the table that C 0 =AB+C 1 (A ⊕B), S=A⊕B ⊕C 1 , so the logic circuit of a binary half adder can be designed in Logisim .

Figure 1-3 is a binary full adder .

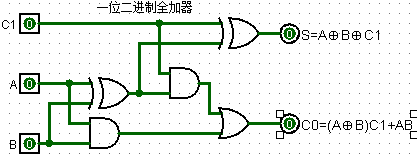


Figure 1-3 One bit binary full adder

**(3) Design scheme of four-bit binary parallel adder with serial carry**

the four-bit binary parallel adder with serial carry , the one-bit binary full adder in the previous question is used for each bit , where A, B come from the corresponding bits of the two operators, and C 1 comes from For the carry of the lower bit , S corresponds to the result of the original bit , and C 0 is used for the lower bit carry of the higher bit . Therefore, four one-bit binary full adders can be connected in series .

Figure 1-4 is a four-bit binary parallel adder with serial carry, which uses a package circuit of a binary full adder .

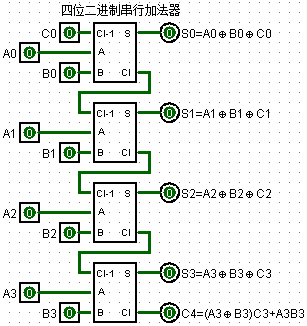


Figure 1-4 serial carry four-bit binary parallel adder

**(4) Design scheme of four-bit binary parallel adder with carry first**

In the carry-first four-bit binary parallel adder , the S and C i of each bit are functions of input A 3 A 2 A 1 A 0 , B 3 B 2 B 1 B 0 and the lowest bit C 0 , rather than The carry C i-1 of the previous bit is irrelevant, that is, the carry of each bit is independent of each other.

S1=P 1 ⊕C 0  S2=P 2 ⊕(P 1 C 0 +G 1 ) S3=P 3 ⊕(P 2 P 1 C 0 +P 2 G 1 +G 2 )

S4=P 4 ⊕(P 3 P 2 P 1 C 0 +P 3 P 2 G 1 +P 3 G 2 +G 3 )

C4=P 4 P 3 P 2 P 1 C 0 +P 4 P 3 P 2 G 1 +P 4 P 3 G 2 +P 4 G 3 +G 4

Figure 1-5 is a four-bit binary parallel adder that carries forward.

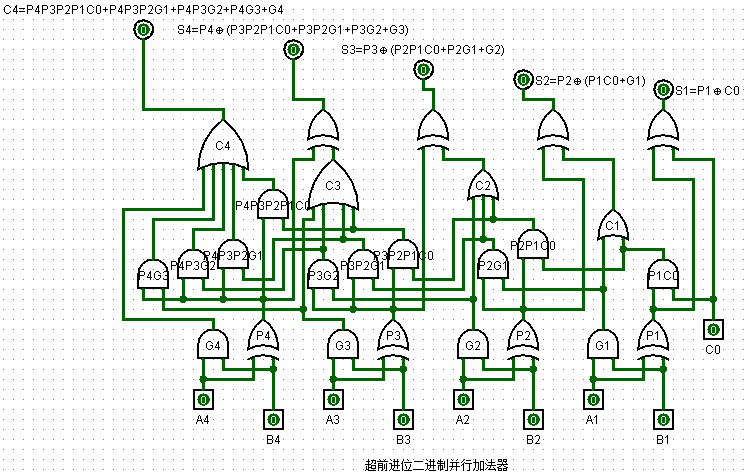
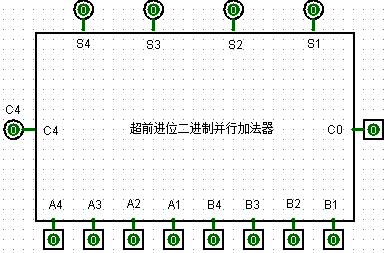


Figure 1-5 Four -bit binary parallel adder with carry ahead

**circuit with carry ahead**

Package the circuit completed in " step 4 " , and then verify the correctness of its design.





**Digital Logic Lab Report**

Small laboratory access control system design experiment report

2. Design of small laboratory access control system

1. Experiment name

Small laboratory access control system design .

2. Purpose of the experiment

Students are required to use traditional circuit design methods to design a logic circuit for a " design scenario " , and use tool software, such as virtual simulation of " logisim " software, to check whether the design of this small laboratory access control system meets the requirements .

Through the three training processes of design , simulation and verification of the above experiments , students can master the design, simulation, debugging methods of small circuit systems and the methods of circuit module packaging .

3. Equipment used in the experiment

of Logisim 2.7.1 software .

4. Experimental content

Design scenario : A small confidential laboratory needs to install an access control system to monitor, control and display the number of people working in the laboratory. The laboratory has only one door and can only accommodate 15 people at most. It is assumed that employees must swipe their campus cards to enter and exit the laboratory, and it is guaranteed that only one person can enter and exit after swiping the card once. When the laboratory is empty, the number of people is displayed as 0, the number of people in the laboratory is increased by 1 when the card is swiped to enter, and the number of people in the laboratory is decreased by 1 when the card is swiped to leave. When the laboratory is full, and there are employees who swipe their cards outside the door to enter, the access control system "does not" act, and the system alarms to indicate that it is full.

Use the logisim software to carry out virtual experiment simulation on small circuits. Except for logic gates, triggers, and 7-segment digital display tubes , the logic component library provided by logisim cannot be used directly . The specific requirements are as follows.

**(1) Design a four-bit binary reversible counter circuit and package and verify its correctness**

a four-bit binary reversible counter with D flip- flop and package it . The counter has a clearing terminal C LR , an accumulative counting pulse terminal CPU ( input swipe card entry request), a cumulative counting pulse terminal CP D (input card swipe away request), four counting output terminals Q D Q C Q B Q A records the current number of laboratory personnel.

the designed 4-bit binary up-down counter to generate a " private " library component for subsequent experiments. The logic symbol of the 4- bit binary up-down counter is shown in Figure 2-1 .

**SD SC SB SA**

**CPU**

**CLR 四位二进制可逆计数器**

**CPD**

Figure 2-1 " private " a 4-bit binary up-down counter

**Design a circuit that converts the number of people in the laboratory into 8421 BCD codes by using the packaged " four-bit binary parallel adder with carry forward " in Experiment 1**

the packaged " four-bit binary parallel adder with advanced carry " and appropriate logic gates in Experiment 1 to convert the number of laboratory personnel represented by binary numbers into 8421 BCD codes of two decimal numbers.

**(3) Design a 7-segment decoder and use a "7-segment digital display tube " to display the circuit of the number of people**

Design a 7-segment decoder (the 7448 chip in the reference book ), and use the "7-segment digital display tube " to display the number of people in the laboratory represented by the 8421 BCD code of two decimal numbers .

The 7-segment decoder has four inputs A 3 A 2 A 1 A 0 and seven outputs abcdefg, A 3 A 2 A 1 A 0 is 8421 BCD code, and abcdefg is the segment corresponding to the 7-segment digital display tube .

**(4) Design the circuit that when the laboratory is full, the access control "does not" act, and the system alarms to prompt full**

When the laboratory is full, the CPU at the accumulative counting pulse end inputs a card swiping entry request, the data at the counting output end remains unchanged, the access control "no" action, and the system alarms to indicate full occupancy. When the laboratory is empty, logically there will be no request to swipe the card to leave the CP D input of the accumulated count pulse terminal in the laboratory. In order to prevent signal interference, when the counting output is 0, if there is a pulse at the CP D terminal, the data at the counting output terminal should also remain unchanged, and the access control "does not" act, but no alarm is required.

**(5) Design a small laboratory access control system circuit and package and verify its correctness**

Design a small laboratory access control system circuit that meets the requirements and package it to generate a small laboratory access control system chip. The logic symbols of the packaged small laboratory access control system are shown in Figure 2-2 .

**十位**：7段数码显示管

**个位：**7段数码显示管

**a b c d e f g a b c d e f g**

**CPU**

**CLR 封装后的门禁系统逻辑符号 报警**

**CPD**

Figure 2 -2 Packaged small laboratory access control system

5. Experimental program design

**(1) Design a four-bit binary up-down counter circuit**

D A = / Q A D B = / Q B D C = / Q C D D = / Q D

CP a = /( CP U ⊕CP D ) CP b =/(CP D /Q A +CP U Q A )

CP c =/(CP D /Q A /Q B + CP U Q A Q B ) CP d =/(CP D /Q A /Q B /Q C + CP U Q A Q B Q C )

Figure 2-3 is a four-bit binary reversible counter circuit.

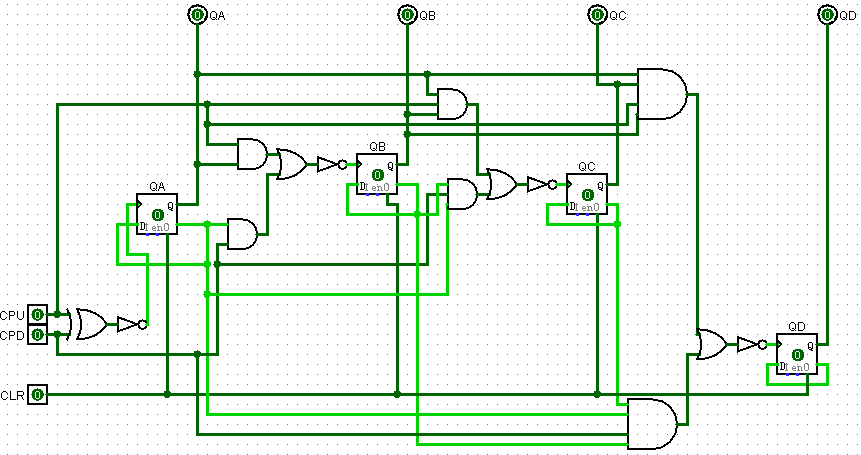


Figure 2-3 A four -bit binary up - down counter

**Design a circuit that converts the number of people in the laboratory into 8421 BCD codes by using the packaged " four-bit binary parallel adder with carry forward " in Experiment 1**

H 4 =H 3 =H 2 =B 3 = B 0 =0; H 1 =C4; A 3 =S4; A 2 =S3; A 1 =S2; A 0 =S1

B 2 =B 1 =(S 4 S 2 +S 4 S 3 )

Figure 2-4 is a circuit for converting a hexadecimal number to 2-digit 8421 code.

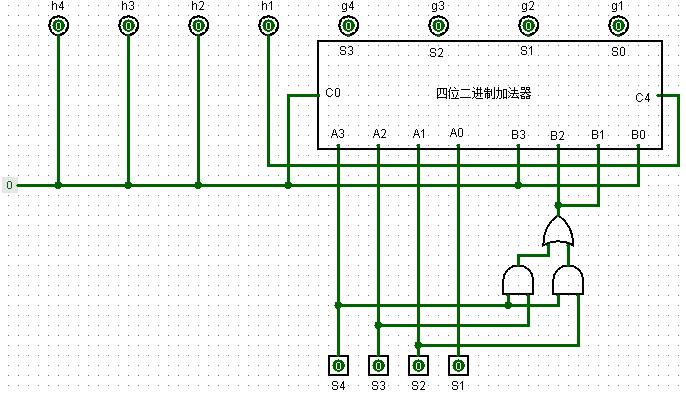
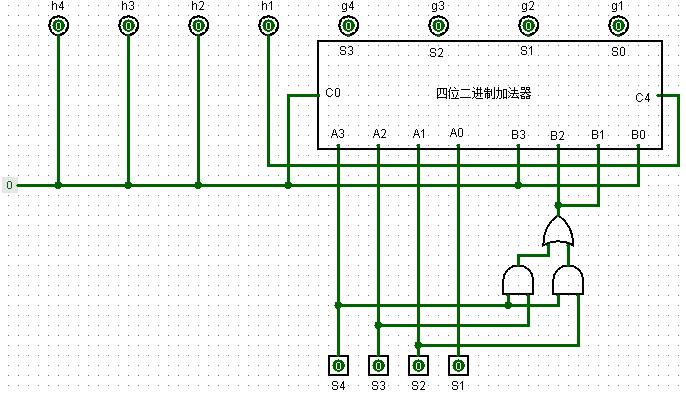


Figure 2 -4 one hexadecimal number converted to two 8421 codes

**(3) Design a 7-segment decoder and use a "7-segment digital display tube " to display the circuit of the number of people**

**( A ) Design a 7-segment decoder**

a=/Q4Q2+/Q4Q3Q1+/Q3/Q2/Q1+Q4/Q3/Q2

b=/Q4/Q3+/Q3/Q2+/Q4/Q2/Q1+Q4Q2Q1

c=/Q3/Q2+/Q4Q1+/Q4Q3

d=/Q3/Q2/Q1+/Q4Q3/Q2Q1+/Q4/Q3Q2+/Q4Q2/Q1

e=/Q3/Q2/Q1+/Q4Q2/Q1

f=/Q3/Q2/Q1+Q4/Q3/Q2+/Q4Q3/Q2+/Q4Q3/Q1

g=/Q4/Q3/Q2+/Q4Q3/Q2+/Q4/Q3Q2+/Q4Q2/Q1

Figure 2 -5 is a 7-segment decoder.

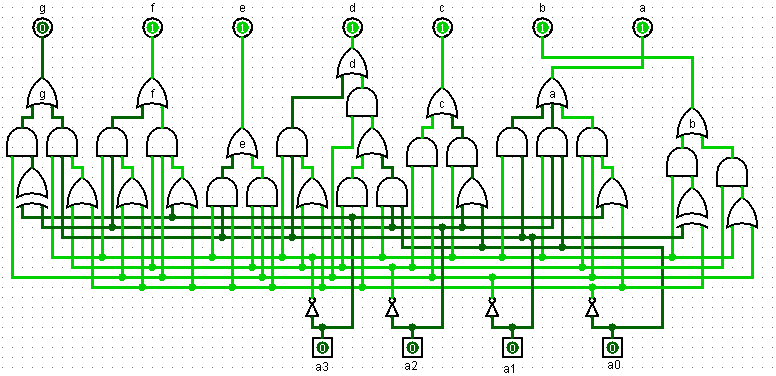


Figure 2-5 7 -segment decoder

**( B ) Design a logic circuit that uses a "7-segment digital display tube " to display the number of people**

Figure 2-6 is a circuit that uses 7-segment digital display tubes to display the number of people in the laboratory .

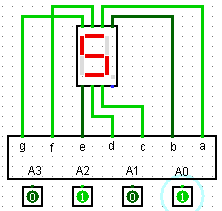


Figure 2-6 uses a 7-segment digital display tube to display the circuit of the number of people in the laboratory

**(4) Design the circuit that when the laboratory is full, the access control "does not" act, and the system alarms to prompt full**

The circuit design requires the use of the " private " library components encapsulated by the 4-bit binary up-down counter in Experiment 1 .

Figure 2 -7 is the alarm circuit .

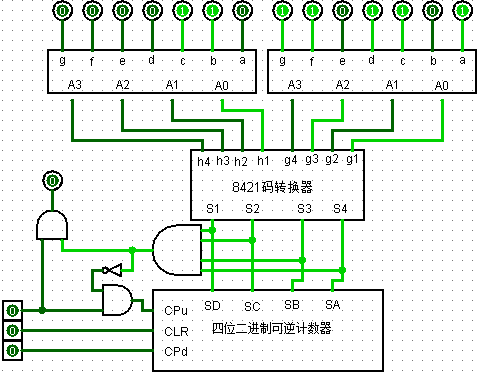


Figure 2-7 alarm circuit

**(5) Design a small laboratory access control system circuit**

Figure 2-8 is the circuit of the access control system .

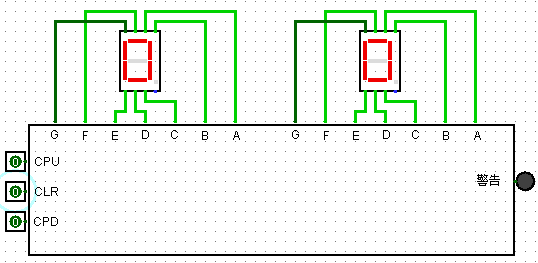


Figure 2-8 Access control system circuit

6. Experimental result record

**(1) Give the test circuit of the " private " library component ( encapsulated with a four-bit binary up -down counter )**

Figure 2-9 is a four -bit binary reversible counter .

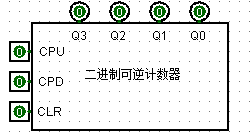


Figure 2-9 A **four -bit binary up-down counter**

**the circuit for converting the number of people in the laboratory into 8421 BCD code designed by using the packaged " four-bit binary parallel adder with carry forward " in experiment 1**

Figure 2-10 is a circuit for converting binary numbers into 8421 BCD codes .



Figure 2-10 The circuit for converting binary numbers into 8421 BCD codes

**the circuit that uses "7-segment digital display tube " to display the number of people**

Figure 2 -11 shows the circuit for the number of people .

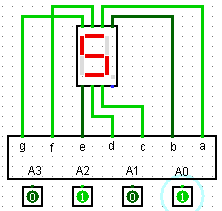


Figure 2-11 The circuit of number display

**(4) Give the circuit that when the laboratory is full, the access control does not operate, and the system alarms to indicate that it is full**

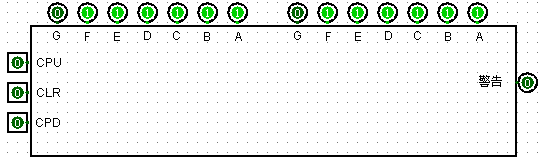


Figure 2-12 is the system alarm circuit

Figure 2-12 system alarm circuit

**the test circuit of the " private " library components (packaged with a small laboratory access control system circuit )**

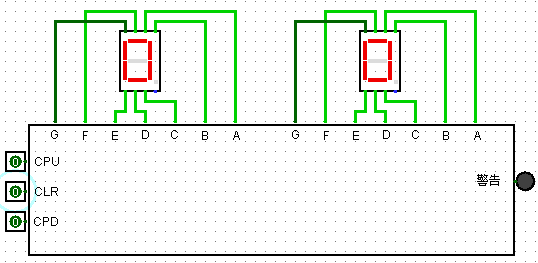


Figure 2 -x is the laboratory access control system circuit

Figure 2-13 Laboratory access control system circuit

7. Thoughts after the experiment

**(1) What do you think are the difficulties of these two experiments ?**

The difficulty I encountered lies in the design of the binary reversible counter and the effective use of the component interface in the conversion to 8421BCD code , that is, the application of the medium-scale general integrated circuit. I still need to use more practice to get familiar with these two design methods .

**(2) How did you solve it ?**

Patiently analyze the function and status, and ask classmates for advice when encountering uncertain places .

**(3) Opinions and Suggestions**

Increase the class hours , and at the same time reduce the degree of difficulty of each design, so as to lay a more solid foundation.